

Form 1449*	Atty. Docket No.: 303.229US2	Serial No. Unknown
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09/12/98
09/12/98
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U. S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
MP	4,394,181	07/19/1983	Nicholas, K.H.	148	1.5	09/28/81
MP	5,145,794	09/08/1992	Kase, M., et al.	437	24	09/06/90
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OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

MP	Berti, M., et al., "Composition and Structure of Si-Ge Layers Produced by Ion Implantation and Laser Melting", <u>J. Mater. Res.</u> , Vol. 6, No. 10, pp. 2120-2126, (1991)
MP	Berti, M., et al., "Laser Induced Epitaxial Regrowth of Si _{1-x} Ge _x /Si Layers Produced by Ge Ion Implantation", <u>Appl. Surf. Sci.</u> Vol. 43, pp. 158-164, (1989)
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MP	Myerson, B.S., et al., "SiGe-Channel Heterojunction p-MOSFET's", <u>IEEE Trans. on Electron Devices</u> , Vol. ED-41, No. 1, pp. 90-100, (Jan. 1994)
MP	Paine, D.C., et al., "The Growth of Strained Si _{1-x} Ge _x Alloys on (100) Silicon Using Solid Phase Epitaxy", <u>J. Mater. Res.</u> , Vol. 5, No., pp. 1023-1031, (1990)
MP	People, R., et al., "Calculation of critical layer thickness versus lattice mismatch for Ge _x Si _{1-x} /Si strained-layer heterostructures", <u>Appl. Phys. Lett.</u> , Erratum, 47, 322, (1985)
MP	Reedy, R., et al., "High Quality CMOS in Thin (100nm) Silicon on Sapphire", <u>IEEE Elect. Device Lett.</u> , Vol. 9, No. 1, pp 32-34, (Jan. 1988)
MP	Wang, K.L., et al., "High Performance GeSi Quantum-Well PMOS on SIMOX", <u>Proc. Int. Electron Device Meeting</u> , San Francisco, pp. 777-778, (Dec. 1992)

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*Substitute Disclosure Statement Form (PTO-1449)

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